

XCS 1000 - Controller Board

OVERVIEW

The XCS 1000 controller board offers an affordable solution of a very flexible, over a large range scalable DSP based board system equipped with the control functions needed to implement controllers for all types of high speed applications. The XCS 1000 has been designed specifically to support complex power electronics control functions.

XCS 1000 is intended for three basic types of applications:

- **Stand-Alone Controllers** for power converters, drives etc.,
- **Rapid Control Prototyping** and
- **Real-Time Simulators.**

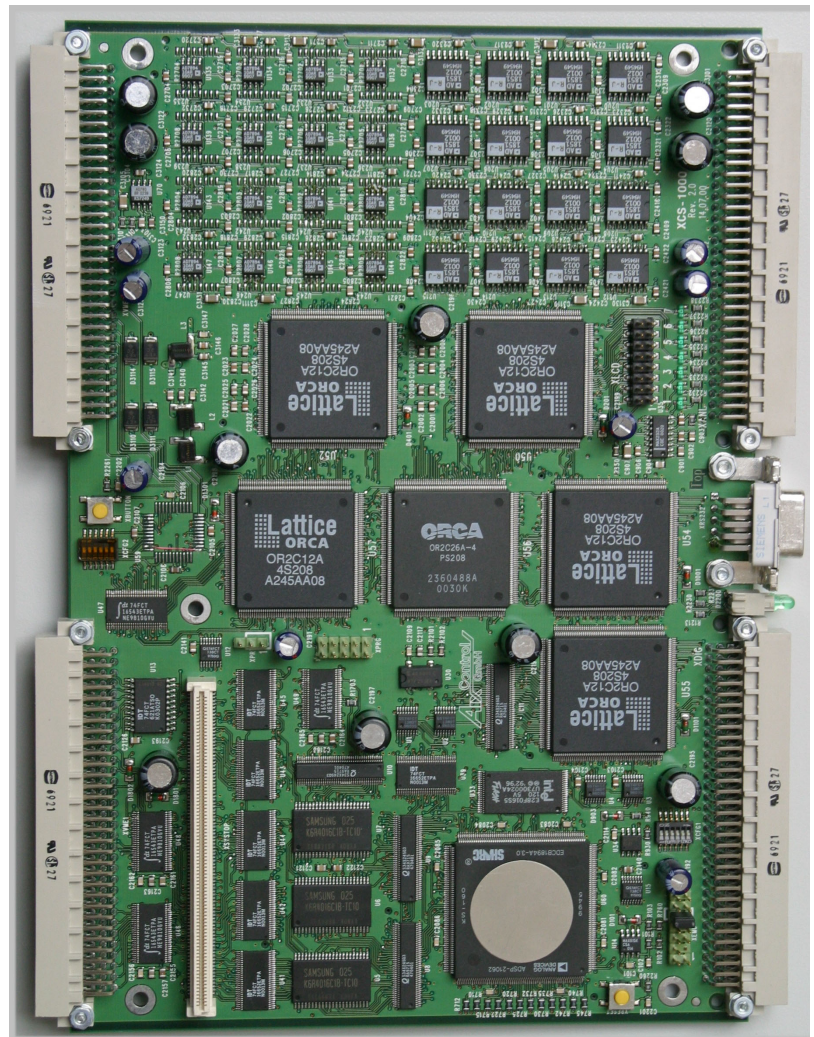
XCS 1000 is especially suitable as a stand-alone controller for any type of control application with additional advantages of floating point and C language support. Special attention was paid to the implementation of control functions for complex power electronic control tasks. Any type of interface can be implemented by the user by reprogramming the FPGAs instead of using the functions provided in the standard hardware. To support Rapid Control Prototyping of power electronic systems, a powerful library exist with numerous I/O- and complex control functions of the XCS 1000.

In addition, a firmware library offers several hardware related interface functions. With the Floating-point-DSP and C-language programming environment easy and fast implementation of algorithms support fastest rapid control prototyping.

Computing power and interfaces of the XCS 1000 board can easily be scaled to meet application requirements. The following basic configurations can be implemented using XCS 1000 boards:

1. Stand-alone single board featuring up to 2 DSPs
 - suitable for stand-alone applications requiring the computing power of one or two DSPs,
 - up to 64 analog and 64 digital I/O channels provided;
2. Stand-alone cluster including up to 3 XCS 1000 boards
 - suitable for applications which require many high-speed I/O channels or fast processing,
 - up to 6 DSPs and up to 192 analog and 192 digital I/O channels provided,
 - fast data exchange and synchronization features among the clustered boards.

Thus, XCS 1000 offers a unique combination of data acquisition capability, a high number of I/O channels, flexible digital interfaces, scalability and high computing power at a reasonable price. XCS 1000 has been optimized to fulfil the requirements of controlling power electronics, drives and industrial automation systems.



KEY FEATURES

Processor

Analog Devices SHARC ADSP-21062
120 MFLOPS peak, 80 MFLOPS sustained performance each at 40 MHz
32/40-Bit precision IEEE/Extended floating-point data formats or 32-Bit fixed-point data format
25 ns instruction rate, single-cycle instruction execution
Integrated multiprocessing feature
Second Processor optional

Memory

2 MBit processor on-chip dual-ported SRAM of each processor for independent accesses by core processor and DMA
256k words of 48-Bit wide fast SRAM for program or data storage
2 MBytes non-volatile Flash EPROM memory for program or data storage
8 kBytes non-volatile Serial EEPROM memory for configuration or data storage

Analog I/O

- Up to 64 simultaneous sampling, memory mapped analog input or output channels, configurable in groups of 4 as input or output individually
- Analog Inputs with 14 Bit resolution at 125 kSamples/sec
- Optional oversampling of up to 1 MSamples/sec on reduced number of inputs
- Analog Outputs with 16 Bit resolution at 3.5 μ sec settling time
- Programmable clocking of analog channels such as simultaneously or consecutively analog input sampling operation
- All analog inputs and outputs buffered via reprogrammable FPGA which can alternatively be used to accommodate digital inputs or outputs

Digital I/O

- 64 memory mapped digital input or output channels, configurable as input or output individually
- Up to 32 individual channels of pulse width modulation

Communication Interfaces

- 2 asynchronous serial RS-232, RS-485 or RS-422 interface channels (max. 8 MBaud)
- DSP interfaces: 4 Link ports and 1 Time-Division-Multiplexed serial port

Flexibility

- All I/O interfaces are implemented using FPGAs, providing a high degree of flexibility
- firmware for standard analog I/O, digital I/O and serial interfaces provided, featuring e.g. PWM channels for power converter control
- Application specific firmware can be implemented by user
- Flexible FPGA-based user programmable interrupt network overcomes the limitation of fixed prioritized external interrupt inputs of the DSPs and interrupts can be shared
- Flexible FPGA-based user programmable hardware synchronization network allows for hardware processes to be synchronized without any load on the DSPs

Extension

- Up to 3 XCS 1000 boards can be stacked together for system extension, Cluster features up to 6 processors, 192 analog and 192 digital inputs or outputs

To accelerate application development and at the same time keep costs low the XCS 1000 concept offers the hard-to-develop key hardware elements of a controller as an affordable standard board produced in large numbers. Application specific functions such as galvanic isolation, attenuation and filtering of input and output signals have to be developed for each application on a simple and fast-to-develop interface board which connects to the XCS 1000 board.

DEVELOPMENT TOOLS

The XCS 1000 board is supported by two sets of software and hardware development tools. One set is provided by Analog Devices. It is specifically designed for the digital signal processor ADSP-2106x. The EZ-ICE In-Circuit Emulator is supported by XCS 1000. Additional information can be found in Analog Devices product information on the SHARC DSP. The other comprehensive set of tools is provided by ISEA and contains DSP-based or PC-based software tools.

The most important DSP-based tool is the boot program which was specifically developed for the XCS 1000 board. It boots the FPGAs prior to both DSPs and external memory and resides in a boot block of the FLASH EPROM. The boot program initializes XCS 1000 using user boot files which are either stored in the FLASH EPROM or accepted via serial interface from a PC or Workstation. Auxiliary DSP-based tools allow to store boot files in the FLASH EPROM.

The most important PC-based tool is a sequence of programs to generate boot files. The XCS 1000 boot file is based on the loader file generated by Analog Devices Development Environment. In addition configuration for FPGAs are included. The flexible interrupt and hardware synchronization networks are supported by comfortable configuration tools.

COMPARISON OF STANDARD VERSION VERSUS MAXIMUM CAPABILITIES

Features	Standard Version	Maximum
Processor	1 ADSP-21062	2 ADSP-21060
Internal Memory	2Mbit per processor	4MBit per processor
SRAM memory words of 48 Bit for program or data storage	256k	1M
Flash-EPROM for program-code and data storage	2 MB	4 MB
Serial EEPROM for configuration and data storage	8 kB	16 kB
Digital Channels, Input or Output	64	64
→ PWM	16	32
Analog Channels, Input or Output	32	64
→ Input-channels:	8 - 24	64
Resolution	14 Bit	14 Bit
→ Output-channels:	8 - 24	64
Resolution	16 Bit	16 Bit
Cluster Extension	yes	yes
TCP/IP-Interface	optional	optional
Delivery time	on stock	8 - 12 weeks

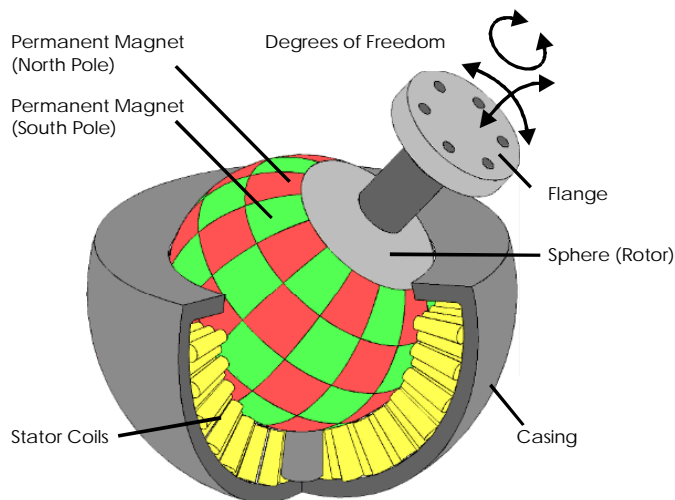
REFERENCE APPLICATIONS

Field Orientation Controller for Induction Machines

- Allows rapid prototyping of new algorithms
- Performs vector-rotation
- Monitors currents and dc-bus-voltage
- Generates PWM-signals at 10 kHz
- 4-times over-sampling for analog values
- Needs no additional control-hardware
- Code written in C language

XCS 1000 Benefits

- Rapid prototyping
- High performance for complex algorithms
- Jitter-free synchronisation among PWM, analog inputs and outputs without any load on DSP



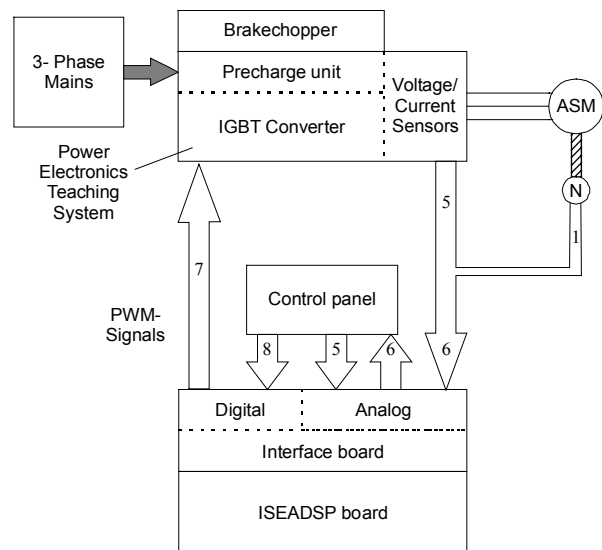
- Large memory for position-force-table

Active Filter

- Compensation of current harmonics
- Rapid Prototyping – several algorithms were compared
- Software phase locked loop, synchronisation to 255 times the line frequency
- Performs sinor-transformation
- Generates analog current command for hysteresis-current-controller
- Code written in Assembly language

XCS 1000 Benefits

- Rapid prototyping
- High performance for complex algorithms

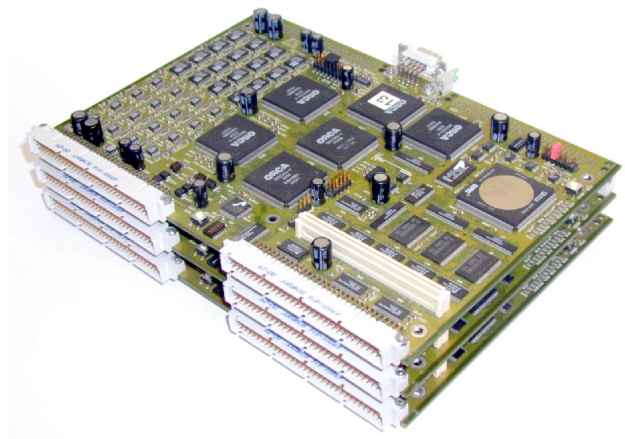


Spherical Motor

- Very complex control of 96 stator currents
- Detailed motor-model performed on second DSP of the same board
- Large position-force-table and interpolation
- LabView-based User-interface via Personal Computer
- Cluster of two boards offers galvanic 96 isolated analog output channels
- Code written in C language

XCS 1000 Benefits

- High number of analog output-channels
- High performance for complex algorithms

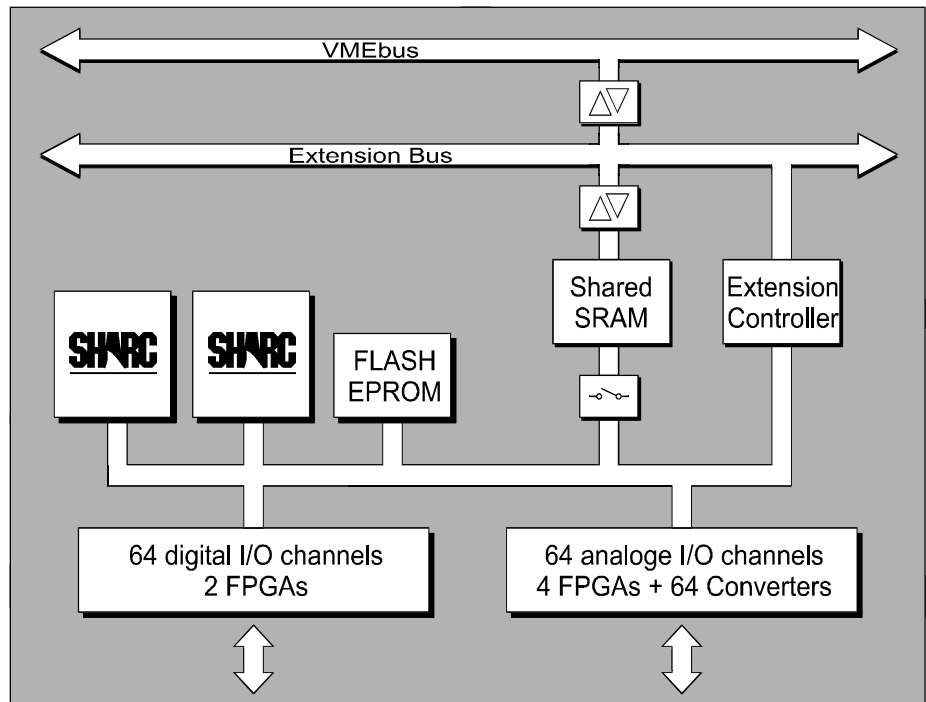


TECHNICAL DESCRIPTION

The XCS 1000 board is constructed as a VME U6-size board which is intended to be used as a stand-alone computer for a wide variety of applications. The functions of each XCS 1000 board can be scaled by populating it according to application requirements. Each XCS 1000 board can be populated with either one or two digital signal processors (Analog Devices SHARC ADSP-2106x) and with up to 64 A/D or D/A converters. To satisfy even higher stand-alone application requirements up to three XCS 1000 controllers, i.e. up to 6 DSPs, can be stacked together into a cluster for system extension with a fixed one master - two slaves configuration.

The XCS 1000 board offers a variety of volatile and non-volatile memory resources. Each processor features up to 4 MBit of internal dual-ported memory for program and data storage. An additional external fast (OWS) static memory can store up to 256k 48-Bit words of program and data.

This static memory serves as a shared RAM between processors and system extension bus. BIOS, FPGA configuration data, processor program as well as user data can be stored in a parallel Flash EPROM of up to 4 MByte of size. The Flash EPROM can be erased partially. Upon power-up the DSPs and the FPGAs are booted from this Flash EPROM. Alternatively, the asynchronous serial interface can be used to boot all devices. A serial EEPROM stores configuration data.



All analog and digital interfaces are memory mapped and controlled by Lucent Technology FPGAs series ORCA2CA. Four analog I/O controller FPGAs control 16 A/D or D/A converters each. Two digital I/O controller FPGAs serve as controllers for 32 digital inputs or outputs each. Alternatively, all six I/O controller FPGAs can serve as application specific digital functions when omitting analog channels.

The main system controller FPGA provides several key functions. Primarily it provides mechanisms to synchronize processes of the DSPs and the FPGAs by programmable interconnect of status and interrupt signals. An example for such a process synchronization would be synchronizing the sampling of A/D converters to PWM power converter gate signals and generating an DSP interrupt upon completion of A/D conversions. In addition, the main system controller supports the asynchronous serial interfaces, the watch dog timer and some useful low level user interfaces such as configurations switches and status LED's.

The system extension controller FPGA manages shared RAM and system extension accesses. This FPGA also features a small dual-ported RAM to allow for conflict free data exchange of master and slave boards. Fast data transfer is achieved via the system extension bus and the shared SRAM's.

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